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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/741,195	12/21/2000	Toshiyuki Hirota	040373/0300	7014

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EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

A/6

Office Action Summary	Application No. 09/741,195	Applicant(s) HIROTA ET AL.	
	Examiner Quang D Vu	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-9,11-16 and 18-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-9,11-16 and 18-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 – 4, 6 – 9, 11 – 16, 18 – 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,326,270 to Lee et al.

Regarding claims 1 and 6, Lee et al. teach a method of manufacturing a semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density, comprising the steps of:

forming a gate oxide film on a surface of the semiconductor substrate (column 1, lines 30-31);

forming gate electrodes (104, 105) on a surface of the gate oxide film, and forming oxide film (110) on the gate electrodes, and forming nitride protective film (106) on the gate electrodes.

uniformly forming a first nitride film (112) having a predetermined thickness on the surface with the gate electrodes formed thereon;

uniformly forming a second nitride film (119) having a predetermined thickness on the surface on which the first nitride film is etched;

self-aligning the high-density region using the first nitride film positioned on sides of the gate electrodes as an etching stopper to form contact holes reaching the semiconductor substrate in the interlayer insulating film;

forming contact electrodes connected to the semiconductor substrate in the contact holes (see figures 3A-G and 4-7).

a method of etching the first nitride film in only the low-density region to expose the gate oxide film in gaps between the gate electrodes (see figure 3B).

forming an interlayer insulating film on the second nitride with an impurity introduced therein on a surface of the second nitride film (column 8, lines 39-40).

Lee et al. do not teach each anneal step as cited in the claimed invention. It is common in the art to perform annealing steps to repair substrate damage, activate dopants, form silicide and other reasons. It would have been a matter of obvious design choice to perform annealing steps at any time during fabrication.

Regarding claims 2, 7, 12 and 19, Lee et al. do not teach the first nitride film and the second nitride film is formed by a CVD. Lee et al. is silent with respect to how the nitride film is deposited. One having ordinary skill in the art would have been required to select a known method of deposition. It would have been obvious to select CVD, as a mater of design choice since it is a well-known method.

Regarding claims 3, 8, 13, 20, 15 and 22, Lee et al. teach a method, wherein the thickness of the first and second nitride films are formed to a thickness of about 20 –200 Angstroms and 50-150 Angstroms, respectively. Lee et al. do not teach a method, wherein the first nitride film is formed to a thickness ranging from 30 to 50 nm, and the second nitride film is formed to a thickness ranging from 3.0 to 20 nm. It would have

been obvious to one having ordinary skill in the art at the time of the invention was made to find the optimal thickness of the first and second nitride film, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art.

Regarding claims 4, 9, 16 and 23, Lee et al. teach a method, wherein the first nitride film is formed to a thickness large enough to serve as an etching stopper for self-aligning the high-density region. Lee et al. do not explicitly teach the second nitride film is formed to a thickness which prevents an impurity of the interlayer insulating film from being diffused into the semiconductor substrate by annealing the assembly in the atmosphere containing the water vapor and also prevents the semiconductor substrate from being oxidized by annealing the assembly in the atmosphere containing the water vapor, but allow the forming gas to be diffused into the semiconductor substrate. It would have been a matter of obviousness for one having ordinary skill in the art to have arrived at an optimal thickness of the second nitride film, as explained in the above paragraph.

Regarding claims 11 and 18, Lee et al. teach a method of manufacturing a semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density, comprising the steps of:

forming a gate oxide film on a surface of the semiconductor substrate;

forming gate electrodes on a surface of the gate oxide film, forming oxide films on the gate electrodes and forming nitride protective films on the gate electrodes;

uniformly forming a first nitride film having a predetermined thickness on the surface with the gate electrodes formed thereon;

etching the first nitride film and gate oxide to expose the substrate in gaps between gate electrodes in said in the low-density region;

uniformly forming a second nitride film having a predetermined thickness on the surface on which the first nitride film is etched;

self-aligning the high-density region using the first nitride film positioned on sides of the gate electrodes as an etching stopper to form contact holes reaching the semiconductor substrate in the interlayer insulating film;

forming contact electrodes connected to the semiconductor substrate in the contact holes (see figures 3A-G and 4-7).

forming an interlayer insulating film on the second nitride with an impurity introduced therein on a surface of the second nitride film (column 8, lines 39-40).

Lee et al. do not explicitly teach a method of etching the first nitride film in only the low-density region to expose the gate oxide film in gaps between the gate electrodes and then removing the gate oxide film in a separate step. Since the etch rates of the gate oxide layer and first nitride film are different, one of ordinary skill in the art would have been required to remove the layers in two etch steps.

Lee et al. do not teach each anneal step as cited in the claimed invention. It is common in the art to perform annealing steps to repair substrate damage, activate dopants, form silicide and other reasons. It would have been a matter of obvious design choice to perform annealing steps at any time during fabrication.

Regarding claims 14 and 21, Lee et al. do not teach a method, wherein the first nitride film is formed by a chemical vapor deposition process, and the second nitride film is formed by a rapid thermal nitriding process. Lee et al. is silent with respect to how the first nitride film is deposited. It would have been obvious to select CVD, as a mater of design choice since it is a well-known method. Rapid thermal nitriding is a well known a method of forming nitride layer. It would have been a matter of obvious design choice to select it.

Response to Arguments

Applicant's arguments with respect to claims 1-4, 6-9, 11-16 and 18-23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 703-305-3826. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Application/Control Number: 09/741,195
Art Unit: 2811

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

QVU
August 9, 2002